25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab3: Transmitter Circuits

Name: Yu-Hao Chen

UIN:435009528

Section:700

Professor: Sam Palermo

TA: Srujan Kumar Kaile

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b. Find the FO4 inverter delay. The bit-rate of transmitters is often limited by the bandwidth of clock buffering. For minimum propagation delay to drive a given capacitive load, a fan-out of four inverter buffer chain (FO4 inverter delay) is often used [5]. Refer to the instructions on how to use the default 90nm CMOS technology models for more details on how to setup the test circuit. For the inverters use minimum channel length and an NMOS unit finger width of 1μm. Size the PMOS/NMOS ratio of the inverter for equal rise and fall delays, measured from 50% of the input to 50% of the output. However, don’t exceed a PMOS/NMOS ratio of 3, i.e., if the simulations show that a ratio greater than 3 is required for equal delay then just use 3 and accept the slight delay difference.

Sweep the supply voltage (VDD) from 0.7V to 1.2V with 50mV step size in order to include FO4 delay [ps] vs. VDD [V].

For the design of half-rate TX architecture, find optimal VDD for maximizing power efficiency at 5Gb/s data rate.

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| FO4 sweep |
| The power |
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Finding the best operation point by power \* FO4 (which is 0.9v)